Hardware Aware Optimization of an Ultra Low Power UWB Communication System

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***Abstract*— A wireless body area network with an average throughput of 500 kbps based on ultra-wideband pulse position modulation is considered. For a long battery autonomy a hardware aware system optimization with respect to the specific applications at hand is essential. A key feature to achieve power savings is low duty cycle signaling, and its effectiveness when combined with burst-wise transmission at high peak data rate. Exploiting this observation, an ultra-low power system is presented, jointly optimized with respect to application and hardware specific aspects. Based on an exhaustive survey of the state of the art literature, its power consumption is estimated significantly below 1 mW.**

I. Introduction

Recently, ultra-wideband (UWB) wireless body area networks (WBAN) gained much interest due to a multitude of attractive applications. In a WBAN, a number of nodes are placed directly on the human body or very close to it. Since WBAN nodes get their power from rechargeable batteries or by energy harvesting, it is inevitable that they are extremely energy efficient. Thus, hardware aware transceiver optimization is essential including parameters such as modulation, multiple access scheme, level of channel state information, duty cycle, frequency band, average and peak data rate, acceptable amplifier non-linearities, sampling rate and digital resolution. In this work, an ultra-low power system is presented enabled by a parameter optimization with respect to one specific WBAN application. The considered application requires an average data rate of $f_{\mathrm{B}} = 500$ kbps, a maximal bit-error-rate of BER $= 10^{-3}$, a maximal latency time of $\tau_{\mathrm{l}} =$1 ms, and a power consumption below 1 mW. Measured WBAN channels show a path loss $PL \leq 60$ dB and a moderate delay spread τ_{rms}=10 ns.

Due to stringent low complexity requirements, an orthogonal binary pulse position modulation (BPPM) is considered combined with an energy detector receiver [1]. The power spectral density of the transmit signal is smoothed by a randomized pulse polarity. In a first stage, only two node communication is considered and a multiple access scheme is avoided, allowing the transmission of one bit per pulse. Beside other parameters, a low duty cycle operation is identified as a key parameter to achieve very low current consumption. In UWB impulse radio (UWB-IR), a low duty cycle is either realized by a low pulse repetition rate or by burst-wise transmission at a high peak data rate with long idle times between the bursts. The later has major practical advantages due to reduced requirements on wake-up time and synchronization precision. Due to the delay spread τ_{rms}=10 ns, the minimal PPM frame duration is restricted to 20 ns and hence, the maximally supported peak data rate equals 50 Mbps. This peak data rate yields a duty cycle of 1% for an average data rate of 500 kbps. To respect the latency time $\tau_{\mathrm{l}} =$1 ms, a burst of 500 bits and 10 μs duration is sent every millisecond. The proposed system achieves an overall current consumption of about 0.45 mA, exploiting the low duty cycle.

The outline of the paper is as follows. The proposed and a reference design model are introduced in Section II and III. The minimal achievable duty cycle and its impact on the overall power consumption are discussed in Section IV and V. Sections VI, VII and VIII treat analog, digital and overall current consumption, respectively, based on an exhaustive literature survey. This is followed by performance results and a short conclusion in Section IX and X.

II. Overview of Proposed Receiver Design

The power consumption of UWB-IR transmitters is small compared to the one of the receivers [2]. Hence, focus is given to the receiver. The transmitter is modeled as a simple BPPM source transmitting bursts of 10 μs every 1 ms at a peak data rate of 50 Mbps and FCC compliant average power of -14.26 dBm at 500 MHz.

A block diagram of the receiver chain is shown in Fig. 1. To realize the analog receiver chain with low complexity resonant circuits, the relative bandwidth of the system should be moderate such that the system can still be considered as narrowband. Hence, the frequency band between $f_{\mathrm{l}} = 3.5$GHz and $f_{\mathrm{u}} = 4$ GHz was chosen to achieve a small path loss as well as small interference from both communication systems around 2 and 5 GHz. First, the receive signal is amplified by a low noise amplifier (LNA) and then filtered by a bandpass. On the one hand, placing the bandpass filter behind the LNA increases the signal-to-noise ratio (SNR) by 5 dB, corresponding to the pass-band attenuation, and allows a significant reduction of duty cycle and power consumption. On the other hand, in-band copies of the out-of-band interference caused by the non-linearity of the LNA are not filtered out. Hence, proposed system sacrifices interference robustness for reduced power consumption and is therefore rather sensitive to

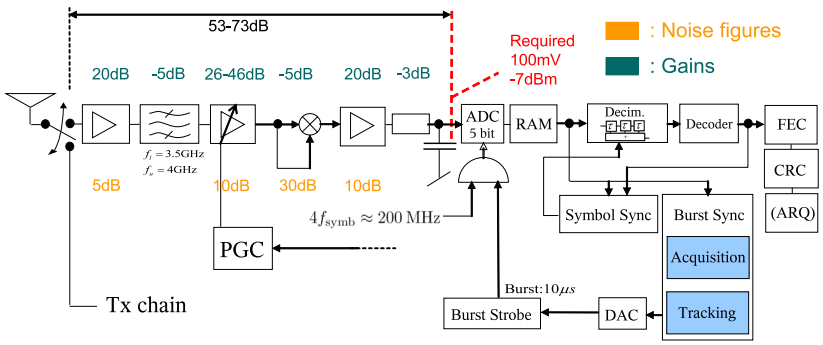

Fig. 1. Block diagram of the UWB-IR receiver

interference. This problem can be circumvented by frequency-selective LNAs [3] or a temporal cognitive multiple access scheme [4]. After the bandpass filter, the signal is amplified by a variable gain amplifier (VGA) controlled by a programmable gain control (PGC), squared and amplified again by a third amplifier. In absence of interference, required IIP3 points of both LNA and amplifiers can be very low. Finally, the signal is low-pass filtered and fed to an analog-to-digital converter (ADC). A simple first order low-pass is used as a replacement for standard integrators that are very power consuming [2]. The ADC contains an integrated amplifier allowing an input voltage range different from the supply voltage. Both power gains and noise figures (NFs) of the individual analog components are indicated in Fig. 1. These are typical values taken from state of the art literature. The PGC tunes the VGA between 26 and 46 dB such that the input amplitude to the ADC stays around 100 mV, where all values are with respect to a nominal (virtual) impedance of 50 Ω. The ADC together with a random access memory (RAM) builds the interface to the digital receiver part. To keep the ADC power consumption small its resolution is set to 5 bits. It is driven by a clock at four times the symbol rate, i.e., at 200 MHz, implying an over-sampling factor $N_{\text{ovsa}} = 4$. The RAM decouples the digital part from the symbol rate and allows burst-wise processing. The output of the RAM is fed to burst and symbol synchronization. Burst synchronization is realized by a pilot based correlation approach that achieves synchronization after a single burst. The symbol synchronization interpolates and down-samples the input signal and thus enables a free-running clock. After the decimator, the decoder consists of a simple subtraction. Forward error correction (FEC), cyclic redundancy check (CRC) code and automatic repeat request (ARQ) control are not specified in the current proposal.

III. Reference Model

A comprehensive overview of a low data rate UWB-IR PPM transceiver, realized in 0.18 μm CMOS technology is given in [2]. Due to its similarity to the proposed system, it is used as reference model. The transmitter consists of a pulse generator driven at 533 MHz, a 33 MHz clock, a delay locked loop, a digital edge combiner, and a transmit filter with pass-band from 3.1 GHz to 4.1 GHz. Peak data rate is 5 Mbps and reported power consumption equals 20 mW at 3.3 V. The receiver chain after the antenna consists of band-pass filter, an LNA, a VGA, a Gilbert-cell mixer and integrators, realized as transconductance amplifiers. For a precise synchronization required for localization, the proposed energy detector is realized as a bank of eight parallel integrators, consuming all together about 68% of the overall power required by the whole analog receiver chain. Hence, there is space for power reduction, if localization is not an issue. Although, the LNA and the baseband block are not specified in the paper, the overall power consumption can be estimated as 116 mW, plus 275 mW for the baseband block [5] and 5 mW for the LNA [6]. This is magnitudes higher than mentioned transmit power consumption.

Another interesting receiver is reported in [3], although realized in a very expensive 90 nm process, with an instantaneous power consumption of 35.8 mW. Based on a turn on time of only 2 ns, the design exploits the low duty cycle by switching of the receiver between subsequent symbols.

IV. Low Duty Cycle Signaling

A $\text{SNR}_{\text{ref}} = 10.5\,\text{dB}$ is required for a BER$= 10^{-3}$ over an Additive White Gaussian Noise channel with BPPM and energy detection. Considering a path loss $PL = 60\,\text{dB}$, an implementation loss $F = 10$ dB, and a thermal noise floor of $N_0 = -174$ dBm/Hz, this corresponds to a transmit energy per bit given by

$$E_{\text{b,tx}} = N_0 + PL + F + \text{SNR}_{\text{ref}} = -93.5\ \text{dBm/Hz}. \quad (1)$$

Hence, the minimal required transmit power to achieve BER$= 10^{-3}$ for a data rate of $f_{\text{B}} = 500$ kbps equals

$$P_{\text{tx}} = E_{\text{b,tx}} + 10\log_{10}(f_{\text{B}}) = -36.5\ \text{dBm}. \quad (2)$$

According to the FCC [7], the average power limit allows to transmit at a power spectral density of $E_{\text{av,max}}$ = -101 dBm/Hz. Thus, the minimal required bandwidth of the considered communication system is given by

$$10\log_{10}(B_{\text{min}}) = P_{\text{tx}} - E_{\text{av,max}} = 64.5\ \text{dBHz} \mathrel{\widehat{=}} 2.8\ \text{MHz}. \quad (3)$$

Increasing the bandwidth B of the communication system, allows to transmit at a higher data rate, while still achieving the required $\text{SNR}_{\text{ref}} = 10.5$ dB. This again allows a reduced duty cycle $\eta = B_{\text{min}}/B = f_{\text{B}}/f_{\text{B,max}}$ according to

$$f_{\text{B,max}} = \tfrac{B}{B_{\text{min}}} f_{\text{B}} = \tfrac{1}{\eta} f_{\text{B}}. \quad (4)$$

To avoid inter-symbol interference (ISI), the BPPM peak data rate is restricted by the delay spread τ_{rms}. Considering typical indoor scenarios, τ_{rms} is in the range of $10 - 50$ ns. Hence, the maximal peak data rate equals [8]:

$$f_{\text{B,max}} \approx \frac{1}{2\tau_{\text{rms}}} \in [10; 50] \text{ Mbps}. \quad (5)$$

Accordingly, the minimum duty cycle, assuming highest peak data rate, equals

$$\eta_{\text{min}} = \frac{f_{\text{B}}}{f_{\text{B,max}}} = \frac{500 \text{ kbps}}{50 \text{ Mbps}} = 0.01 = 1\%. \quad (6)$$

Respecting a maximal latency time τ_{l} =1 ms, $N_{\text{bit}} = 500$ bits per millisecond are buffered into one data burst and transmitted at 50 Mpbs within 10 μs, still providing an average data rate of $f_{\text{B}} = 500$ kbps. At the expense of 100 times more bandwidth, the signaling scheme allows a duty cycle of 1% and hence, the transceiver can stay in sleep mode during 99% of the time. Ideally, the power consumption could be reduced by a factor of 100.

Due to a fixed system bandwidth of 500 MHz and a corresponding FCC compliant average power of -14 dBm, there is a clear trade-off between duty cycle reduction and link margin. While the link margin for a 1% duty cycle is just 2.5 dB, it increases to 9.5 dB for a duty cycle of 5%.

In compliance to the FCC, switching on and off a high data rate system is called gating. As the FCC allows the emitted power of a gated systems to be measured in normal operation mode including silent phases, the transmit power of the 1% duty cycle signal can be increased by approximately 14 dB. Accordingly, the link margin is increased.

V. Energy Consumption Analysis

Typical current consumptions of existing wireless communication systems are 20 mA at 0.1 Mbps for ZigBee, 30 mA at 0.3 Mbps for Bluetooth, 100 mA at 10 Mbps for WLAN and 200 mA at 100 Mbps for Wireless USB. Hence, it can be expected that the current consumption scales sub-linearly with the data rate, which is confirmed in this section. The following energy consumption analysis is split into an analog and digital part, as they behave differently with respect to the clock frequency.

A. Energy Consumption of Analog Integrated Circuits

The model for the current consumption of the analog receiver front end assumes a constant behavior with respect to data rate. For a given supply voltage V_{dd}, the energy consumption scales linear with the current according to $E_{\text{analog}} = V_{\text{dd}} T_{\text{burst}} I_{\text{analog}}$. This relationship states that reducing the duty cycle η, i.e., the on-time ηT_{burst} of the analog front end, directly relates to energy saving.

B. Energy Consumption of Digital Integrated Circuits

In CMOS circuits there are generally four major sources of power dissipation [9]. Leakage and standby current are clock frequency independent. Leakage current is caused by a reverse bias current in the parasitic diodes between source (drain) and bulk in an MOS transistor, and by subthreshold current. The standby current corresponds to the direct current from V_{dd} to ground, when pMOS and nMOS transistors are continuously on. In this work, we consider 0.18 μm CMOS technology or larger. With respect to more advanced technologies as 90 or 65 nm, this choice has the advantage of reduced production costs and the possibility to co-integrate analog and digital parts. With 0.18 μm CMOS technology driven below 1 GHz, leakage and standby current can be neglected.

Short circuit and capacitance currents dominate the current consumption in well-designed CMOS circuits and depend on the clock frequency. The short circuit current arises due to non-zero rise and fall times of the input waveforms, during which there exists a direct path between V_{dd} to ground. The capacitance current is the necessary current to charge and discharge capacitive loads during logic changes. This is the dominant current flow in digital CMOS circuits.

Summarizing, the model for the energy consumption of the digital part leads to

$$E_{\text{digital}} = V_{\text{dd}} T_{\text{burst}} I_{\text{digital}} = V_{\text{dd}} T_{\text{burst}} \left(I_{\text{digital,0}} + k f_{\text{s}} \right), \quad (7)$$

where $I_{\text{digital,0}}$ models the clock frequency independent part, k the clock frequency dependent current consumption per digital operation cycle, and f_{s} is the clock sampling frequency. Usually the clock independent part can be neglected, i.e., $I_{\text{digital,0}} = 0$.

C. Energy Consumption for Duty Cycle Signaling

We introduce the duty cycle signaling with T_r, the time required by the analog part and the digital part to receive, store and process the data. According to the previous section, it is assumed that $I_{\text{digital,0}} = 0$ and that the digital part of the receiver can start to process the data already after a few samples are stored to the RAM. The energy consumption of the analog part and the digital part are captured in E_{analog} and E_{digital}, respectively. Hence, the overall energy consumption equals:

$$E_{\text{total}} = E_{\text{analog}} + E_{\text{digital}} \quad (8)$$

with

$$E_{\text{analog}} = V_{\text{dd}} T_{\text{r}} I_{\text{analog}} \quad (9)$$

$$E_{\text{digital}} = V_{\text{dd}} k f_{\text{s}} T_{\text{burst}} = V_{\text{dd}} k N_{\text{ovsa}} N_{\text{bit}}, \quad (10)$$

where $N_{\text{bit}} = 500$ is the number of bits per burst, N_{ovsa} is the over-sampling factor according to $f_{\text{s}} = N_{\text{ovsa}} f_{\text{B,max}}$. We consider the fraction of energy consumption $\zeta(\eta)$ for duty cycle ($T_{\text{r}} = \eta T_{\text{burst}}$) over the energy consumption for full duty cycle ($T_{\text{r}} = T_{\text{burst}}$)

$$\zeta(\eta) = \frac{E_{\text{total}}(\eta)}{E_{\text{total}}(1)} = \frac{\eta + \gamma}{1 + \gamma} \quad (11)$$

with

$$\gamma = \frac{k N_{\text{ovsa}} N_{\text{bit}}}{T_{\text{burst}} I_{\text{analog}}}. \quad (12)$$

Thus, the amount of energy, which can be saved by using low duty cycle signaling depends on γ, which relates clock frequency dependent to clock frequency independent current consumption. Using the current consumption per digital operation cycle $k = I_{\text{digital}}/f_{\text{s}}$, one achieves:

$$\gamma \approx \frac{I_{\text{digital}} N_{\text{ovsa}} N_{\text{bit}}}{I_{\text{analog}} f_{\text{s}} T_{\text{burst}}}, \tag{13}$$

where I_{digital} is the current consumption of a digital circuit for a given sampling frequency f_{s}, i.e., the current for f_{s} operation cycles. Typical numbers for I_{analog} and I_{digital} are presented in Section VI and VII based on state of the art values.

VI. The Analog Components and Their Power Consumption

In this section, the results of an exhaustive literature survey with respect to typical power consumptions of the proposed analog RF components are presented. Presented state of the art components not always match perfectly to proposed component parameters but are sufficiently close for a robust and precise estimation of the power consumption. Although, the ADC and the clock build the edge between analog and digital part, we will consider their power consumption in this section.

A. Low Noise Amplifier

An LNA with frequency range $3.4 - 6.9$ GHz, a 10 dB gain, and a noise figure smaller than 10 dB is reported [10] with a power consumption of 3.5 mW at a supply voltage of 1 V. Another LNA [11] with range $2 - 10$ GHz, 13 dB gain, and a noise figure below 3.3 dB, requires a power consumption of 9.5 mW at 2.4 V. Due to its target frequency range $2 - 4.6$ GHz and its realization in 0.18 μm CMOS technology, the design in [6] seems very suited. The proposed LNA has a gain of 9.8 dB and a noise figure of only 2.3 dB. Having an IIP3 of -7 dBm, the power consumption is 12.6 mW at 1.8 V, i.e., the current consumption is 7 mA. Considering different values from literature, the power consumption of the LNA is estimated to be $I_{\text{LNA}} = 5$ mA.

B. Amplifier

For convenience, it is assumed that both VGA and amplifier are realized the same way. Appropriate amplifiers have been found in literature with power consumptions in the range between 8.1 and 15 mW and currents between $3.2 - 8.3$ mA [2], [12], [13]. Due to its realization in 0.18 μm CMOS as well as its target frequency range 3.1-4.8 GHz, the amplifier in [14] seems the most appropriate solution. This amplifier consumes 25 mW at 1.8 V, i.e., about 13.9 mA. Its 1 dB compression point lies at -22 dBm and hence, the IIP3 at about -12 dBm, which is sufficient in case of no interference. No noise figure is mentioned. Considering the different values from literature, the current consumption of the amplifier is approximated with $I_{\text{Amp}} = 5$ mA.

C. Squaring Device

By guaranteeing a sufficiently large signal level at the input of the squaring device, it is realized as a mixer with the same input signal on both inputs. Similar current consumptions of about $I_{\text{Mix}} = 1.5$ mA are reported in [2], [15], [16], which is taken as a reasonable estimate.

D. Analog-to-digital Converter and Clock

In literature, three interesting ADCs with 5 bit resolution and a sampling frequency above 200 MHz have been found. Due to its realization in 0.18 μm CMOS, the one presented in [17] seems very close to the requirements. It operates at a sampling rate of 500 MHz, and requires 1 mW at 1.2 V in the analog part and 6.5 mW at 1.8 V in digital domain, leading to an overall power consumption of 7.5 mW. The ADC in [18] operates at 600 MHz and requires 28.5 mW at 3 V. Our reference design requires only 2 mW at 3.3 V. A current consumption of about $I_{\text{ADC}} = 3$ mA seems a reasonable estimate for an ADC with a sampling rate of 200 MHz.

The required 200 MHz clock is generated by a quartz crystal of 40 MHz multiplied by a phase-locked-loop (PLL) circuit requiring an overall current of $I_{\text{s}} = 5$ mA.

E. Overall Analog Current Consumption

With the filters realized as passive elements, summing up the different current consumption values from above leads to the overall current consumption of the analog receiver part:

$$I_{\text{analog}} = I_{\text{LNA}} + 2 \cdot I_{\text{Amp}} + I_{\text{Mix}} + I_{\text{ADC}} + I_{\text{s}} \approx 24.5 \text{ mA} \tag{14}$$

for a 100% duty cycle. However, the analog current consumption scales with the duty cycle. Assuming a 1% duty cycle, the current consumption falls to $I_{\text{analog}} \approx 0.24$ mA.

VII. The Digital Part and its Power Consumption

For an estimation of the digital power consumption, the system complexity is evaluated in terms of additions and multiply-and-accumulates (MAC) per bit. Combined with published values for RAM, standard adders and MACs this leads to an estimation of the overall power consumption of the digital part.

A. Complexity Estimation

As mentioned in Section II, the decoder consists of a simple substraction. Hence, most complexity of the digital part arises from storage, burst and symbol synchronization. The burst synchronization is split into an initial phase, an acquisition phase and a tracking phase. The initial phase equals synchronization from scratch, such as after a system shut down, where the burst has to be found within a window of 1 ms. This is the most complex synchronization phase, but it can be neglected, as it is performed only very seldom. The acquisition phase occurs after a communication break, where rough knowledge about the burst's location is still available. Tracking is performed from burst to burst. Generally, the acquisition phase consists of finding a pilot burst in an uncertainty window of length $T_{\text{ac}} = N_{\Delta,\text{ac}} T_{\text{burst}}$ with $N_{\Delta,\text{ac}}$

a constant, describing the synchronization uncertainty. This is the same as finding a sequence of length $N_{\text{ovsa}}N_{\text{bit}}$ in a window of $N_{\Delta,\text{ac}}N_{\text{ovsa}}N_{\text{bit}}$ samples. For each correlation test, $(N_{\text{ovsa}}N_{\text{bit}})/2$ additions are required to add up the energy from the expected PPM slots. Assuming $N_{\Delta,\text{ac}} = 3$ and an acquisition phase every $N_{\text{ac}} = 100$ burst, e.g., after an interference, the number of required additions per data bit is $C_{\text{add,ac}} = (N_{\Delta,\text{ac}}N_{\text{ovsa}}^2N_{\text{bit}}^2)/(2N_{\text{ac}}N_{\text{bit}}) = 120$ samples/bit. During the tracking phase, a pilot sequence of length $N_{\text{tr}} = 8$ is prepended $N_{\Delta,\text{tr}} = 3$ times at the start of each burst. Hence, the correlation at the receiver requires $C_{\text{add,tr}} = (N_{\Delta,\text{tr}}N_{\text{ovsa}}^2N_{\text{tr}}^2)/(2N_{\text{bit}}) = 3$ samples/bit.

The complexity of the symbol synchronization based on a three-tap FIR filter and a four-times over-sampled signal is estimated to $C_{\text{MAC,symb}} = 3 \cdot 4 = 12$ MAC/bit. Collecting numbers the overall complexity per bit is estimated to 124 additions and 12 MACs. The last addition comes from the decoder.

B. Random Access Memory (RAM)

The RAM decouples the digital signal processing part from the ADC clock. Due to the over-sampling factor $N_{\text{ovsa}} = 4$, it works at 200 MHz and requires a minimal memory size of 2.5 kb. For the considered design, static RAMs (SRAM) are more interesting, as they are generally faster and more power efficient than dynamic RAMs (DRAM). In [19], a number of different SRAMs with their active mode power consumption are presented. All of them are realized by a 0.25 μm process. Depending on memory size and access time, the reported power consumption lies in the range between 3.6 and 63.8 mW. Another low-power SRAM [20], realized in a 0.25 μm CMOS process, with a chip size of 256 kb and a clock rate of 200 MHz requires 26 mW read and 28 mW write power at 2.5 V. The SRAM presented in [21] fits our system best with respect to chip size and access time and especially, its realization in 0.18 μm CMOS. In normal mode, the presented 4 kb SRAM works at a clock rate of 250 MHz and consumes an average power of 23.2 mW at a supply voltage of 1.8 V. Its access time equals 3.38 ns. During standby mode the average power is reduced to 0.11 mW. All chips are still larger than the required memory size. Hence, for the realization at hand a smaller power consumption can be expected. Based on presented values, the current consumption of an SRAM with reduced bit resolution operated at 200 MHz is estimated to be 10 mA during active mode and 0 mA during standby.

C. Full Adder

We consider the full adder that has three inputs, i.e., both summands and carry, and two outputs, i.e., sum and carry. In [22], the authors compare different adders realized in a 0.35 μm process. They require a normalized current consumption of about 21 nA/MHz. Recently, low-power full adders were presented in [23]. One presented CMOS realization has a power consumption of 3.8 μW at 0.8 V and 50 MHz, i.e., 76 nW/MHz. Based on the above values, a current consumption of about 70 nA/MHz for a full adder seems to be a rather conservative estimate.

D. Multiplier-Accumulator

Beside some high-speed MAC structures, a low-power MAC is presented in [24]. Using a clock speed of $f_{\text{s}} = 22$ MHz and a 16×16 bit resolution, 352 M MAC/s can be processed with a power consumption of 14 mW at 1.5 V. Thus, 25 M MAC/s/mW are possible with a 16×16 bit resolution. For considered system, a 8×8 bit resolution is sufficient with 25 M MAC/s at an estimated power consumption of 0.25 mW.

E. Overall Digital Current Consumption

The overall complexity of 124 additions and 12 MACs per bit was determined in Section VII-A. According to [23], 50 M additions/s can be performed with a power consumption of 3.8 μW. In one second, $124 \cdot 500$ k = 62 M additions are required to fulfill the data rate constraint of 500 kbps, corresponding to $f_{\text{s}} = 2$ MHz. This is about 1.2 times higher than the capacity provided by this structure [23]. Assuming a linear scaling, the power consumption scales to 4.5 μW at 0.8 V, i.e, 5.6 μA. Due to the required data rate of 500 kbps, $12 \cdot 500$ k MAC/s = 6 M MAC/s have to be processed. The structure presented in Section VII-D, requires 0.25 mW for 25 M MAC/s. This is about 4 times more than required. Hence, the power can be decreased by this factor leading to a power consumption of about 63 μW at 1.5 V, i.e, 42 μA. Hence, the overall current consumption of adders and MACs is dominated by the MAC operations, and approximated with 48 μA for 500 kbps and a sampling clock of $f_{\text{s}} = 2$ MHz. To incorporate read and write operations over different busses, this number is doubled to 96 μA.

As discussed further above, the average current consumption of the RAM is estimated to 10 mA, when constantly operated at 200 MHz. However, the RAM is roughly operated at 1% of the time, requiring only 0.1 mA. This corresponds to the current consumption required for operating the RAM at 500 kbps, i.e., $f_{\text{s}} = 2$ MHz, and 100% duty cycle. Hence, the overall current consumption of the digital part equals $I_{\text{digital}} = 196$ μA at 2 MHz or I_{digital} =19.6 mA at 200 MHz.

VIII. Overall Power Consumption

To evaluated the overall power saving of the low duty cycle system, the estimated current consumptions I_{analog} =24 mA and I_{digital} =19.6 mA at 200MHz, are plugged into (13) together with $N_{\text{ovsa}} = 4$, $N_{\text{bit}} = 500$, $f_{\text{s}} = 200$ MHz, and T_{burst} =1 ms. With these values a γ of 0.008 is obtained and ζ is given by $\zeta(\eta) = (\eta + 0.008)/1.008$. Finally, for an expected duty cycle of $\eta = 0.01$ the fraction of used energy equals $\zeta = 0.018$. Thus, we can save roughly 98% of the energy, when we operate our system at a duty cycle of 1%. The overall current consumption of the system roughly equals 0.45 mA. In this work, the times for switching off and on the system were neglected, but should not exceed a few microseconds.

IX. Performance over Multi-Path Channels

Performance results are presented over UWB ear-to-ear channels from two different persons measured in an anechoic chamber, whereby, the ear-to-ear link is considered as a typical WBAN link with an average path loss of 60 dB. Results are based on a hardware aware BER simulation environment incorporating discussed system parameters and imperfections according to Fig. 1. Most important are non-linear LNA and amplifier models, noise figures, 5-bit ADC resolution and non-adaptive symbol synchronization. In Fig. 2, the corresponding BER curves are plotted over transmit power P_{tx}. It is apparent and encouraging that with the maximal allowed FCC transmit power of about 0 dBm a link margin of 11 dB is achieved. Hence, proposed ultra-low power communication system for WBAN application works.

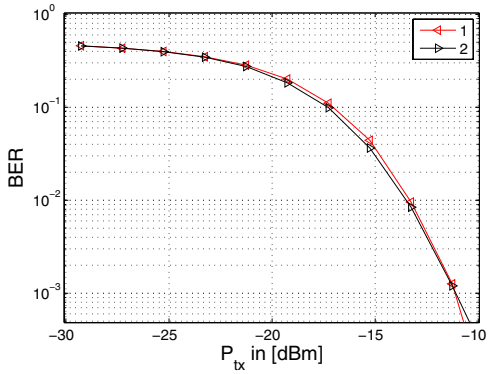

Fig. 2. BER curves plotted over transmit power P_{tx}

X. Conclusions

A UWB-IR ultra-low power communication system was optimized with respect to a specific WBAN application incorporating hardware aspects. It is demonstrated that presented low duty cycle system is capable of operating with an average power consumption significantly less than 1 mW, which seems unreached by state of the art systems. This is done by an exhaustive literature survey and a theoretic estimation of the system's current consumption as a function of the duty cycle. Based on a realistic simulation environment, the principal feasibility of the link was demonstrated with respect to BER.

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